ABSTRACT

The present invention discloses a method and system for synchronizing processing modules. More specifically the present invention utilizes a master clock signal and associated synchronization information to coordinate the function dictated by packets within a synchronization stream. The master clock has multiple sources. Each module in the system is connected to each clock source to ensure that if one source fails, the module will not fail. The clock signal to each module is further passed through a locked oscillator, which will continue to maintain the clock signal should the master clock signal fail. Each module contains a sync decoder to decode the SYNC packets in the synchronization stream, into system time events. The system time events are then passed to a plurality of event receivers. Each event receiver contains at least one flywheeling counter to ensure that each event receiver remains in synchronization with the system time events being passed by the sync decoder. Flywheeling also permits receivers to remain synchronized in the absence of the synchronization stream for finite periods of time.